Amendments to the Drawings

Figures 4A- 4C and 5A - 5C have been revised to include the designation "Prior Art." Figure 4A has been revised to include a label for the node "output" and a capacitor "C" from output to ground, consistent with the circuit operation as described in Figures 4B and 4C and in the text of the specification.

Figure 7D has been revised to label the two voltage levels V1+Vdd and V2+Vdd, consistent with the description in specification paragraph 0034.

Replacement sheets for Figures 4A - 4C and 5A - 5C are attached at the end of this paper as an appendix.

REMARKS

I. Status of Claims

Claims 1-20 stand rejected.

II. Objection to Drawings per MPEP § 608.02(g)

The examiner has objected to Figures. 4A- 4C and 5A-5C in that they should be designated by a legend such as --Prior Art-- because only that which is old is illustrated.

Revised drawings designating Figures 4A-4C and 5A - 5C as prior art are attached to this paper as an appendix.

III. Objection to Claim 16.

The examiner correctly noted that claim 16 should depend from claim 12, not claim 1. Claim 16 has been amended to depend from claim 12.

IV. Claim Rejections - 35 USC § 112

The examiner has rejected claims 1-20 under 35 U.S.C 112, first paragraph, as based on a disclosure which is not enabling.

Claim 1 recites a digital to analog converter coupled to the oscillator for generating an analog signal of predetermined voltage level based on the pumping signal as configured by a set of inputs thereof; and a charge pump coupled to the DAC for producing a dc output based on the analog signal. The examiner has alleged that "the disclosure does not properly enable one of ordinary skill in the art to understand

how one or more analog signals of predetermined voltage level are generated or how a dc output based on those analog signals is generated."

The applicant has revised Fig. 4A to label the "output" node and to correct an omission of an output capacitor "C" that was inconsistent with Figures 4B and 4C and the text of the specification. One of ordinary skill in the art would have understood from the text and Figures 4B and 4C that the output capacitor, C, must be present in Figure 4A. No new matter is added. As depicted in the revised Fig. 4A, the circuit comprises a prior art charge redistribution D/A converter, which produces a variable output voltage pulse (Fig. 4C) depending on which switches (a, b, . . . n) are closed. Operation of a conventional charge redistribution digital to analog converter as illustrated in Figure 4 A is well-known in the art and described, for instance in 'Principles of Data Conversion System Design,' 1995 ISBN -07803-1093-4 by Behzad Razavi, pp. 63-70, 74-77, and in US Patent 4,451,820, Charge Redistribution Integratable D/A Convertor by Kapral." A copy of the Razavi reference is attached to this paper.

The examiner has further alleged that "the DAC shows only one output whereas the charge pump requires two inputs CLK and CLKB. The applicant has amended the specification paragraph 0030 to clarify that "charge pump 500 . . . receives <u>two</u> pumping signals from two D/A converters such as the one shown in Figure 4A, wherein the output pulses of the D/A converters are 180 degrees out of phase with each other." This description is consistent with the following statement in the original paragraph

that "These two pumping signals are oppositely biased square waves CLK and CLKB." The circuit in Figure 5A is well known in the art as a means to invert a DC voltage.

The examiner has also alleged that "the nature of the signals 316 is unknown" and "the specification provides no explanation as to the nature of module 304's construction or function." As amended, paragraph 0025 of the specification clarifies the nature of signal 316, which is a binary signal if the D/A converter 306 has binary-weighted charge redistribution capacitors (as shown in Fig. 4A) or thermometer-weighted signal if the charge redistribution capacitors are all of the same value. One of ordinary skill in the art would have understood from the circuit diagram of Fig. 4A that a binary-weighted digital input would be used with the D/A converter if the capacitors were binary weighted as shown in Figure 4A and that thermometer-weighted digital signals would be used if the charge redistribution capacitors were all of the same value. No new matter us added. Thermometer-weighted digital signals are well known in the art of digital to analog conversion and an explanation of the conversion that would be done in code converter 308 if a binary to thermometer conversion is needed can be found in the Razani reference that has been attached to this response.

The examiner has stated that "the nature of the signals output from module 304 is unknown." As clarified in paragraph 0025, the output of module 304 is a clocked, i.e. duty-cycled, binary (or thermometer-weighted) digital signal. One of ordinary skill in the art, familiar with charge redistribution D/A convertors would have recognized from Fig. 4a that the inputs to the D/A converter required clocked binary or

thermometer weighted digital signals and that module 304 combined the ring oscillator and the digital signals 316 to create clocked digital signals. No new matter is added.

Claims 1, 12 and 17

The examiner has alleged "It is not clear toward what the "one of more outputs" recited in claim 1 line 8 is directed," and raised similar questions with independent claims 12 and 17. All independent claims now refer to only a single analog voltage output.

Claim 11

Claim 11 recites "wherein the charge pump is a voltage doubler producing the output as a sum of a voltage output swing of the D/A converter and a supply voltage." The examiner has stated that "No voltage doubler has been disclosed" because "the output voltage from 704 is not doubled, but is the sum of a varying input voltage and a fixed voltage Vdd." The circuit configuration of module 704 as described as a "voltage doubler" is a well-known configuration in the art. In the mode employed here, where the clock signal into the "doubler" is not a clocked version of the supply voltage, but is a clocked signal that varies up to the supply voltage, the output of the "doubler" is technically only double when the output of the D/A converter 702 is 100% of the power supply voltage. Nevertheless, the description of the circuit topography as a voltage doubler is appropriate, and the remainder of the claim makes clear, consistent with the specification that the output is "a sum of a voltage output swing of the D/A converter

and a supply voltage." Figure 7D has been revised consistent with the description in the specification to show voltage levels of V1+Vdd and V2+Vdd.

In light of the remarks and explanations above, the examiner's rejections regarding enablement have been overcome. The applicant requests that the rejections be withdrawn and the claims allowed as amended.

V. Claim Rejections - 35 USC § 102

The examiner has rejected Claims 1, 4, 5, 10 &11 under 35 USC 102(b) as being anticipated by Chow (6,002,699). Claim 1 states

> a digital to analog (D/A) converter coupled to the oscillator for generating an analog signal of a predetermined voltage level based on the pumping signal as configured by a set of inputs thereof;

Chow does not disclose "a digital to analog (D/A) converter coupled to the oscillator for generating an analog signal of a predetermined voltage level based on the pumping signal as configured by a set of inputs thereof." Contrary to the examiner's assertion, element 31 in Fig. 5 of Chow, the "adaptive swing clock generator" does not function as the D/A converter in claim 1. Chow does not disclose inputs to element 31 that can be adjusted to configure the analog signal output. To the contrary, Chow discloses a "closed loop circuit with negative feedback . . . which ultimately settles into a steady-state condition." Column 4, lines 37-39. Moreover claim 1 recites a "digital to analog converter." Chow does not disclose any digital input to element 31, therefore element

31 cannot be considered a "DAC." The output voltage in Chow is set by "the voltage division ratio of [a] voltage divider," not digital inputs. Column 5, lines 30-32.

For the reasons stated above, the applicant asserts that the examiner's § 102 rejection based on Chow of claim 1 and the claims that depend from claim 1 have has been overcome, and requests that the rejection be withdrawn.

VI Claim Rejections - 35 USC § 103

The examiner has rejected Claim 2 under 35 USC § 103(a) as being unpatentable over Chow in view of Katsuhisa (USPN 6,762,640). Claim 2 recites "the generator of Claim 1 further comprising a load capacitor coupled to the charge pump." Because Katsuhisa fails to cure the deficiencies of Chow with respect to the features of claim 1 and 2, i.e. that Chow does not disclose nor suggest a D/A converter, and it would not have been obvious to include a D/A converter in Chow because Chow does not disclose or suggest digital inputs the applicant has overcome the examiner's rejection of claim 2/

The examiner has rejected claims 3, 6, 12, 14, 16, 17 and 20 under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Komiya et al (USPN 6,714,065). Each of these claims either recites or depends from a claim that recites "a digital to analog (D/A) converter coupled to the oscillator for generating an analog signal." Komiya fails to cure the deficiency of Chow described above in that Chow does not disclose a digital to analog converter. Komiya does not disclose or suggest the addition of a D/A

converter. Therefore none of claims 3, 6, 12, 14, 17 or 20 would have been obvious based on Chow and Komiya.

The examiner has rejected claims 13 and 18 under 35 USC § 103(a) as being unpatentable over Chow in view of Komiya et al. and Katsuhisa. Because Chow does not disclose a D/A converter, and Komiya and Kaysuhisa fail to cure this deficiency, neither claim 13 nor 18 would have been obvious based on Chow in view of Komiya et al. and Katsuhisa.

For the reasons stated above, the applicant asserts that the examiner's rejection of claims 2, 3, 6, 12-18 and 20 under 35 USC §103(a) has been overcome and requests that the rejection be withdrawn and the claims allowed.

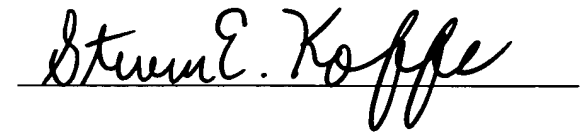
IV. Conclusion

Having addressed the examiner's rejections, applicant submits that the reasons for the examiner's rejections of Claims 1-20 have been overcome. Applicant respectfully requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued.

Should any unresolved issues remain, the examiner is requested to call Applicant's attorney at the telephone number below.

The Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may be associated with this communication to Duane Morris LLP deposit account 04-1679.

Respectfully submitted,



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